GUIDELINES:
Distribution of periods :

No. of classes required to cover JNTU syllabus	:	40
No. of classes required to cover Additional topics	:	4
No. of classes required to cover Assignment tests (for every 2 units 1 test)	:	4
No. of classes required to cover tutorials	:	8
No. of classes required to cover Mid tests	:	2
No of classes required to solve University Question papers	:	4
Total periods		6

14. Detailed notes

UNIT 1
INTRODUCTION

Synthetic detail of an integrated circuit through four layers of planarized copper interconnect, down to the polysilicon (pink), wells (greyish), and substrate (green).

Integrated circuits were made possible by experimental discoveries which showed that semiconductor devices could perform the functions of vacuum tubes and by mid-20th-century technology advancements in semiconductor device fabrication. The integration of large numbers of tiny transistors into a small chip was an enormous improvement over the manual assembly of circuits using electronic components. The integrated circuit's mass production capability, reliability, and building-block approach to circuit design ensured the rapid adoption of standardized ICs in place of designs using discrete transistors.

There are two main advantages of ICs over discrete circuits: cost and performance. Cost is low because the chips, with all their components, are printed as a unit by photolithography rather than being constructed one transistor at a time. Furthermore, much less material is used to construct a packaged IC die than a discrete circuit. Performance is high since the components switch quickly and consume little power (compared to their discrete counterparts) because the components are small and positioned close together. As of 2006, chip areas range from a few square millimeters to around 350 mm^2, with up to 1 million transistors per mm

IC Fabrication Process:

An integrated circuit consists of a single crystal chip of
silicon. Containing both active and passive elements, and their interconnection.

The basic structure of an IC consists of four layers of materials, such that:

1.Substrate
2.Epitaxialgrowth
3.Diffusion
4. Metallization

Substrate:

The p-type silicon bottom layer (6 mils thick) and serves where the Integrated circuit is to be built known as Substrate.

Epitaxial growth:

The second n-type layer (25μm=1mil) where all active and passive component are built, which is grown as a single crystal extension is called Epitaxial growth.

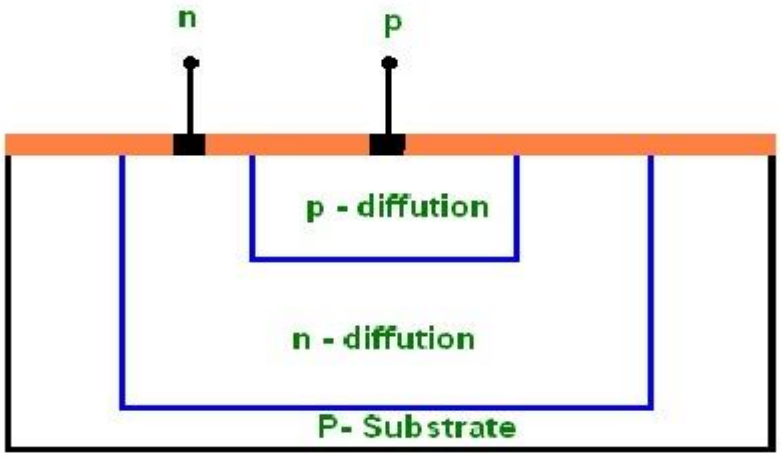
Diffusion:

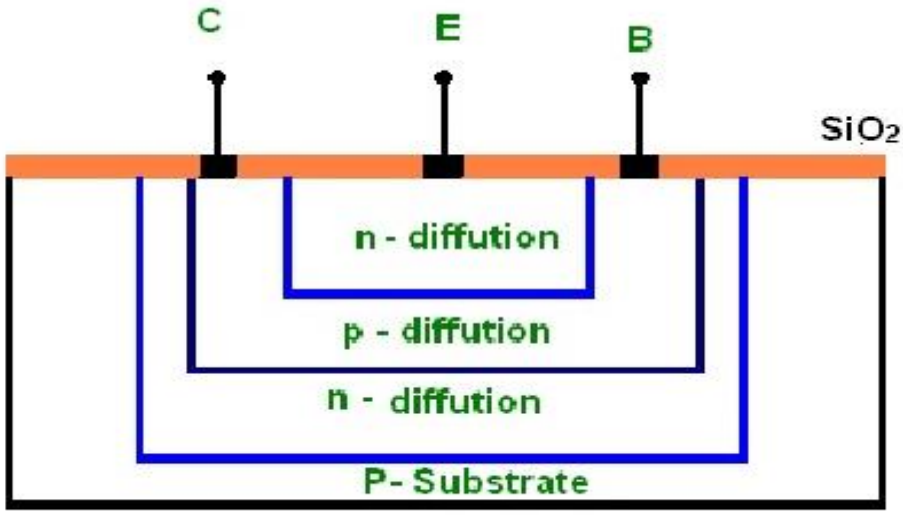
The third layer of IC fabrication is Diffusion process. Active and passive component are made by diffusing p-type and n-type impurities. The selective diffusion of impurities is accomplished by using SiO_2 as a barrier.

Metallization:

Finally a fourth material (aluminum) Layer is added to supply the necessary interconnection between components. It provided contact among the components Al is used for metallization.

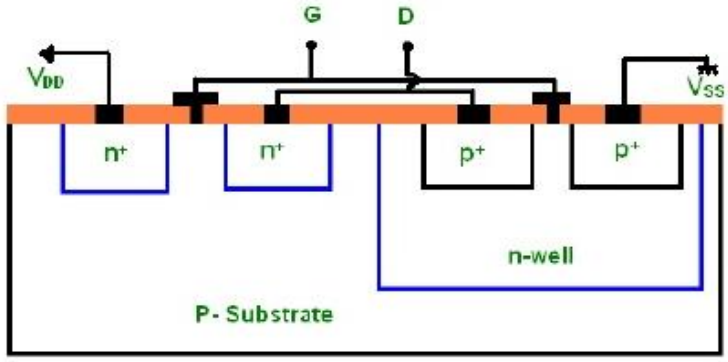
Diode Fabrication:

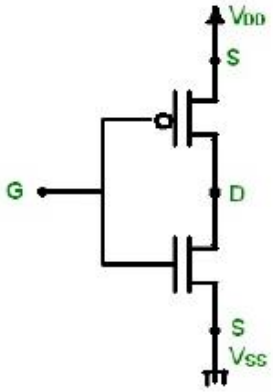




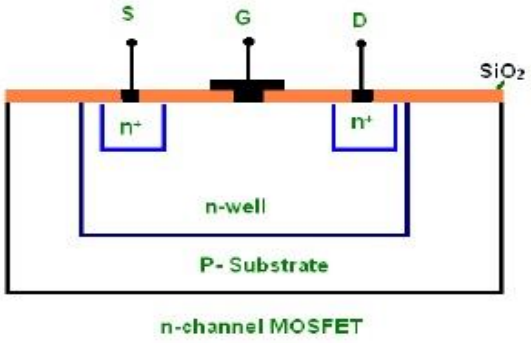
Transistor Fabrication:

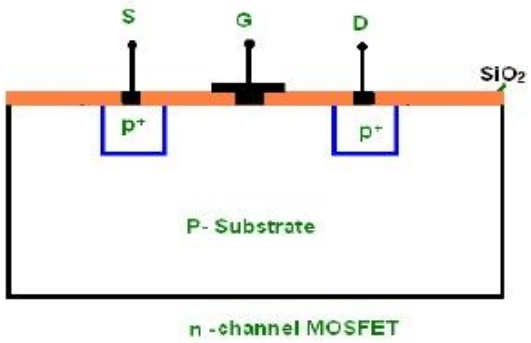
CMOS:
Fabrication:



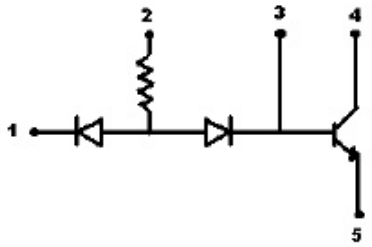


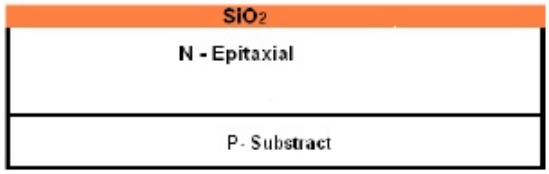
MOSFET Fabrication:

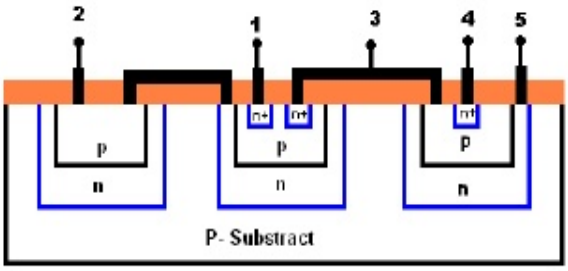


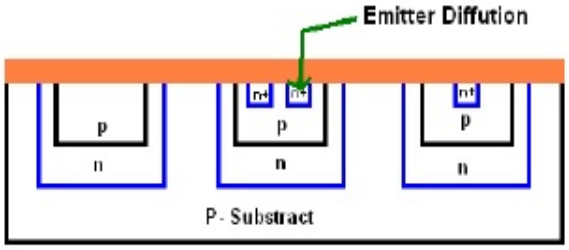


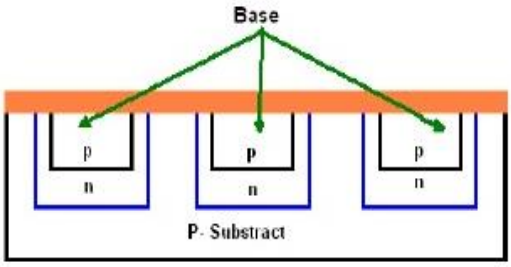
Monolithic IC:

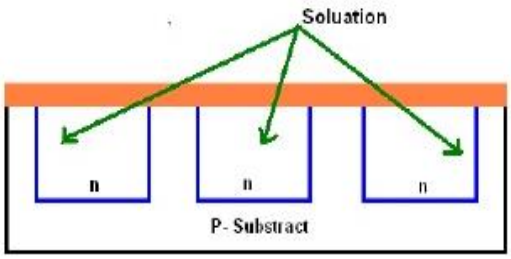












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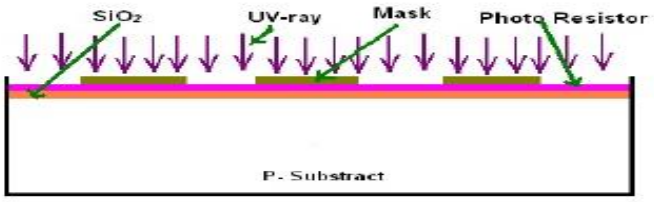
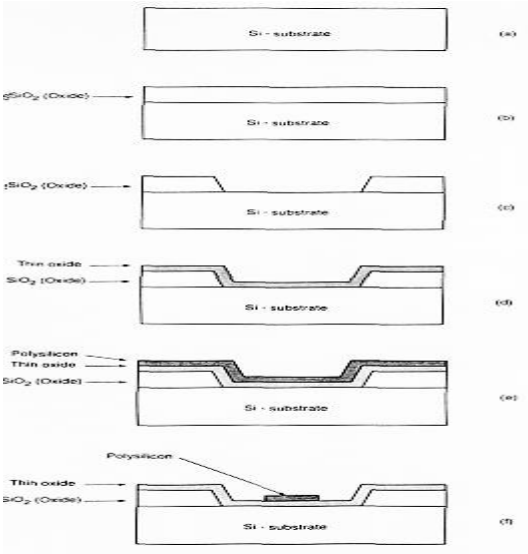
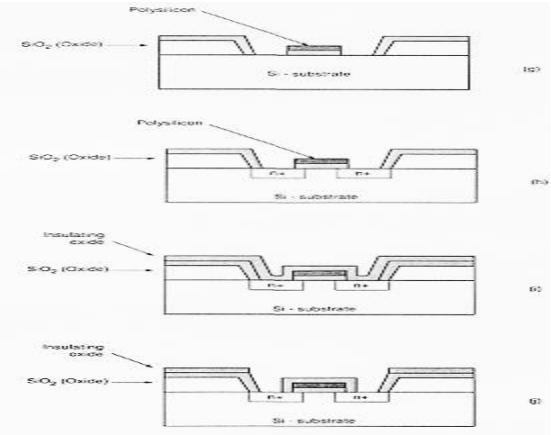


Fabrication process:



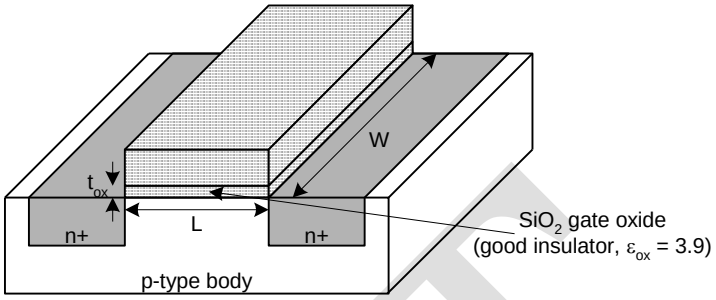


IC characteristics / Elimination:

1. Typical value of Resistance 10Ω < R < 30 kΩ & Capacitance <30pf.
2. Poor tolerance typical value is 10% only.
3. High thermal co-efficient & voltage resistive.
4. No transfer & inductor can be fabricated.
5. Higher cost for small scale production.

BASIC ELECTRICAL PROPERTIES

The MOS transistor evolves from the use of a voltage on the gate to induce a charge in the channel between source and drain, which may then be caused to move from source to drain under the influence of an electric field created by voltage Vds applied between drain and source. Since the charge induced is dependent on the gate to source voltage then Ids is dependent on both Vgs and Vds.



MOS structure looks like parallel plate capacitor while operating in inversion

– Gate – oxide – channel

Qchannel = CV

C = Cg = eoxWL/tox = CoxWL

$V = V_{gc} - V_t = (V_{gs} - V_{ds}/2) - V_t$

Charge is carried by e-

Carrier velocity *v* proportional to lateral E-field between source and drain

v = mE m called mobility

E = Vds/L

Time for carrier to cross channel:

t = L /V

Now we know

How much charge Qchannel is in the channel

How much time t each carrier takes to cross

$$I_{ds} = \frac{Q_{channel}}{\beta} = \mu C_{ox} \frac{W}{L}$$

$$= \mu C_{ox} \frac{W}{L}\left(V_{gs} - V_t - V_{ds}/2\right)V_{ds}$$

If Vgd < Vt, channel pinches off near drain, When Vds > Vdsat = Vgs – Vt

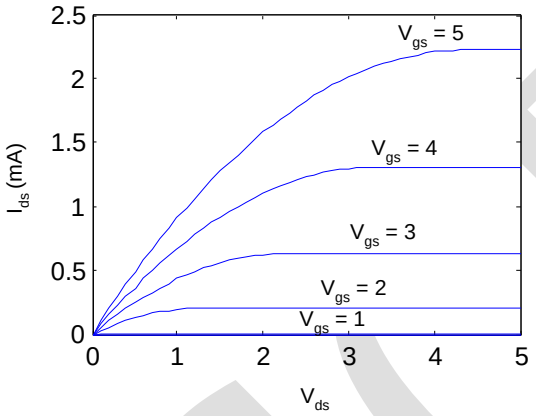
Now drain voltage no longer increases current

$$I_{ds} \equiv \beta\left(V_{gs} - V_t - V_{dsat}/2\right)V_{dsat}$$

$$= \frac{\beta}{2}(V_{gs} - V_t)^2$$

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \quad \text{cutoff} \\ \beta\left(V_{gs} - V_t - V_{ds}/2\right)V_{ds} & V_{ds} < V_{dsat} \quad \text{linear} \end{cases}$$

Characteristics of nMOS transistor:



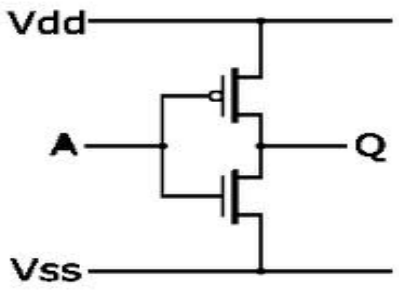
MOS Transistor threshold voltage:

The **threshold voltage** of a MOSFET is usually defined as the gate voltage where an inversion layer forms at the interface between the insulating layer (oxide) and the substrate (body) of the transistor. The purpose of the inversion layer's forming is to allow the flow of electrons through the gate-source junction.

FIGURE OF MERIT:

A **figure of merit** is a quantity used to characterize the performance of a device, system or method, relative to its alternatives. In engineering, figures of merit are often defined for particular materials or devices in order to determine their relative utility for an application. In commerce, such figures are often used as a marketing tool to convince consumers to choose a particular brand.

CMOS INVERTER:



This is a CMOS inverter, a logic gate which converts a high input to low and low to high. Click on the input at left to change its state. When the input is high, the n-MOSFET on the bottom switches on, pulling the output to ground. The p-MOSFET on top switches off. When the input is low, the gate-source voltage on the n-MOSFET is below its threshold, so it switches off, and the p-MOSFET switches on to pull the output high

Inverting Amplifier :

Push-pull inverter

Large signal analysis

VTC and Inversion voltage.

Compare with the earlier VTC.

Small signal analysis

Gain = Vout/Vin= - (gm1+ gm2)/(gds1 + gds2)

Rout = Vout/Iout|Vin=0 ≅ 1/(gds1 + gds2)

CMOS Inverter analysis :

Inverter Threshold (midpoint, inversion) Voltage(VI) :

point of intersection of VTC and unity gain line.

Inverter design 1: DC Design :

- To design the value of VI for a particular VTC

Compute the design parameter from the expression of VI.

Calculate the value of VI for inverter having same aspect ratio (W/L)n = (W/L)p

Inverter design 2: Transient Design :

The transient response should be symmetrical with tLH=tHL.

but once (W/L)n and (W/L)p are decided the time constants are also determined.

DC design sets the general shape of the switching waveforms

High performance design

To achieve smaller time delays in digital signal path

Cout= Cint + CL,

Cint : internal MOSFET capacitance and is dependent on

device aspect ratio.

CL: external load capacitance due to large no of fan-out.

Large aspect ratio (W/L) is to be chosen for design to achieve fast charging and discharging of Cout..

Trans conductance:

Transconductance, also known as **mutual conductance**, is a property of certain electronic components. Conductance is the reciprocal of resistance; transconductance, meanwhile, is the ratio of the current change at the output port to the voltage change at the input port. It is written as g_m. For direct current, transconductance is defined as follows:

$$g_m = \frac{\Delta I_{\text{out}}}{\Delta V_{\text{in}}}$$

PASS TRANSISTOR:

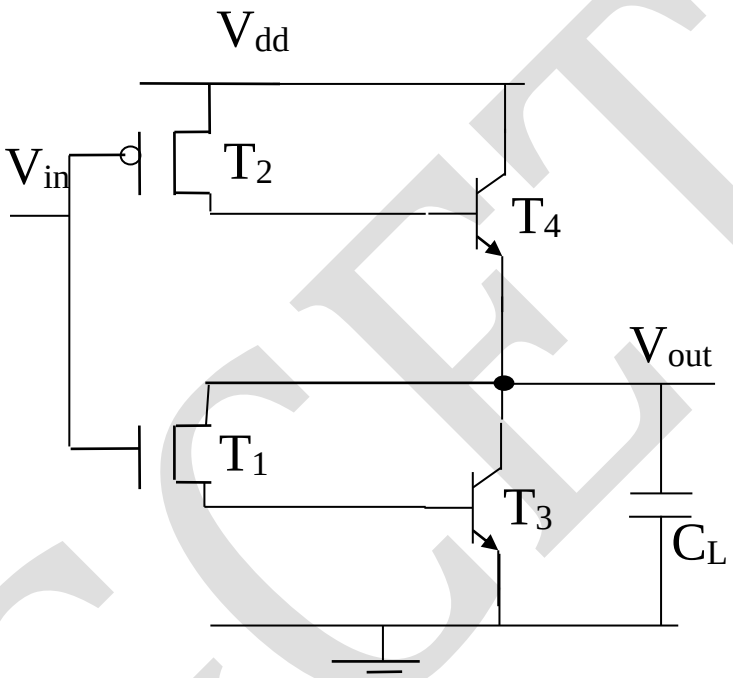
In electronics, **pass transistor logic** (PTL) describes several logic families used in the design of integrated circuits. It reduces the count of transistors used to make different logic gates, by eliminating redundant transistors. Transistors are used as switches to pass logic levels between nodes of a circuit, instead of as switches connected directly to supply voltages. This reduces the number of active devices, but has the disadvantage that output levels can be no higher than the input level. Each transistor in series has a lower voltage at its output than at its input. If several devices are chained in series in a logic path, a conventionally-constructed gate may be required to restore the signal voltage to the full value. By contrast, conventional CMOS logic always switches transistors to the power supply rails, so logic voltage levels in a sequential chain do not decrease.

BICMOS INVERTER:

BiCMOS is an evolved semiconductor technology that integrates two formerly separate semiconductor technologies - those of the analog bipolar junction transistor and the digital CMOS transistor - in a single integrated circuit device.

Two bipolar transistors (T3 and T4), one nMOS and one pMOS transistor (both enhancement-type devices, OFF at Vin=0V)

The MOS switches perform the logic function & bipolar transistors drive output loads



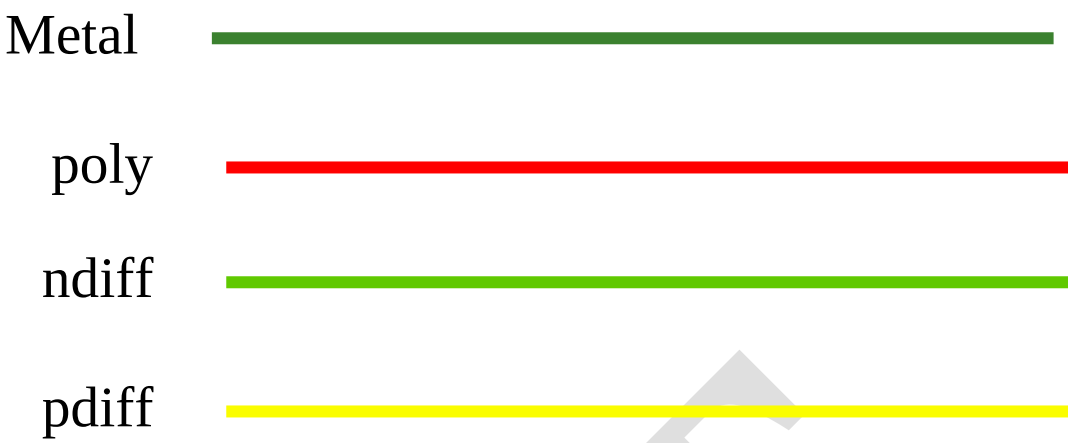
UNIT 2

VLSI CIRCIUT DESIGN PROCESSES

MOS design is aimed at specification into masks for processing silicon to meet the specification .MOS circuits are formed on four basic layers –n-diffusion, p-diffusion, polysilicon and metal, which are isolated from one another by thick or thin(thinox)silicon dioxide insulating layers. The thin oxide (thinox) mask includes n=diffusion, p-diffusion and transistor channels.

STICK DIAGRAM:

Stick diagrams are used yo convey the information through the use of a color code .the below table shows the color code



- Allow translation of circuits (usually in stick diagram or symbolic form) into actual geometry in silicon
- Interface between circuit designer and fabrication engineer
- Compromise
  - designer - tighter, smaller
  - fabricator - controllable, reproducible

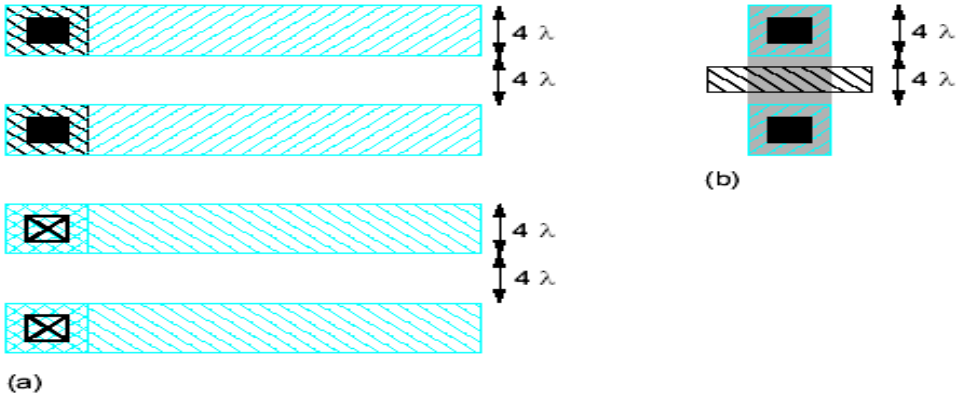
Lambda Based Design Rules :

Design rules based on single parameter, λ

- Simple for the designer
- Wide acceptance
- Provide feature size independent way of setting out mask
- If design rules are obeyed, masks will produce working circuits
- Minimum feature size is defined as 2 λ
- Used to preserve topological features on a chip
- Prevents shorting, opens, contacts from slipping out of area to be contacted

Wiring:

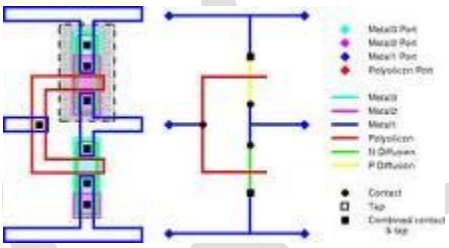
wiring is the space required for a wire
4 λ width, 4 λ spacing from neighbor = 8 λ pitch
Transistors also consume one wiring track



Design Rules :

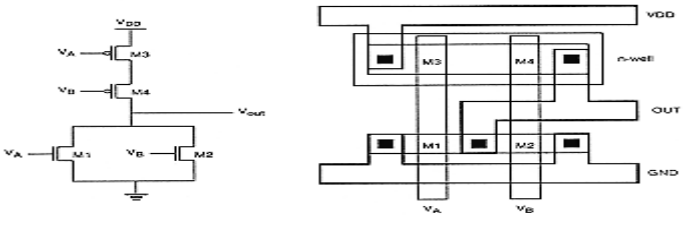
- Manufacturing processes have inherent limitations in accuracy and repeatability
- Design rules specify geometry of masks that provide reasonable yield
- Design rules are determined by experience

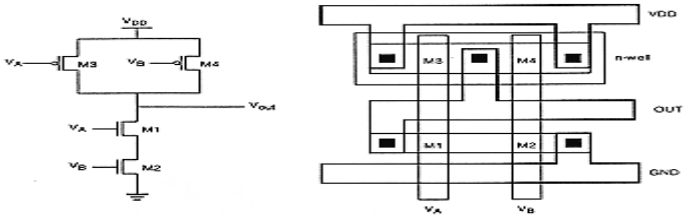
Nmos stick diagram:



Layout of CMOS NAND and NOR Gates:

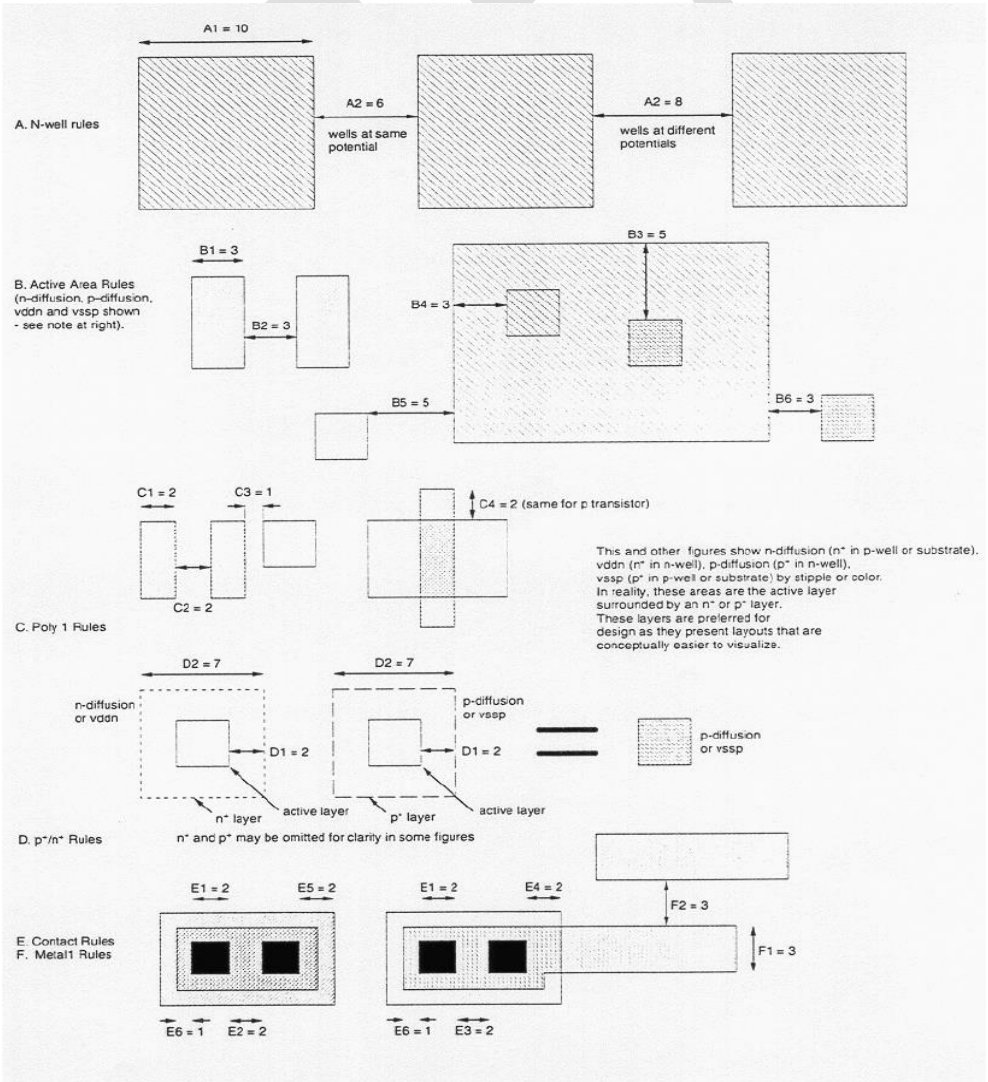
The mask layout designs of CMOS NAND and NOR gates follow the general principles examined earlier for the CMOS inverter layout. Figure 3.7 shows the sample layouts of a two-input NOR gate and a two-input NAND gate, using single-layer polysilicon and single-layer meta.





CMOS Layout Design Rules:

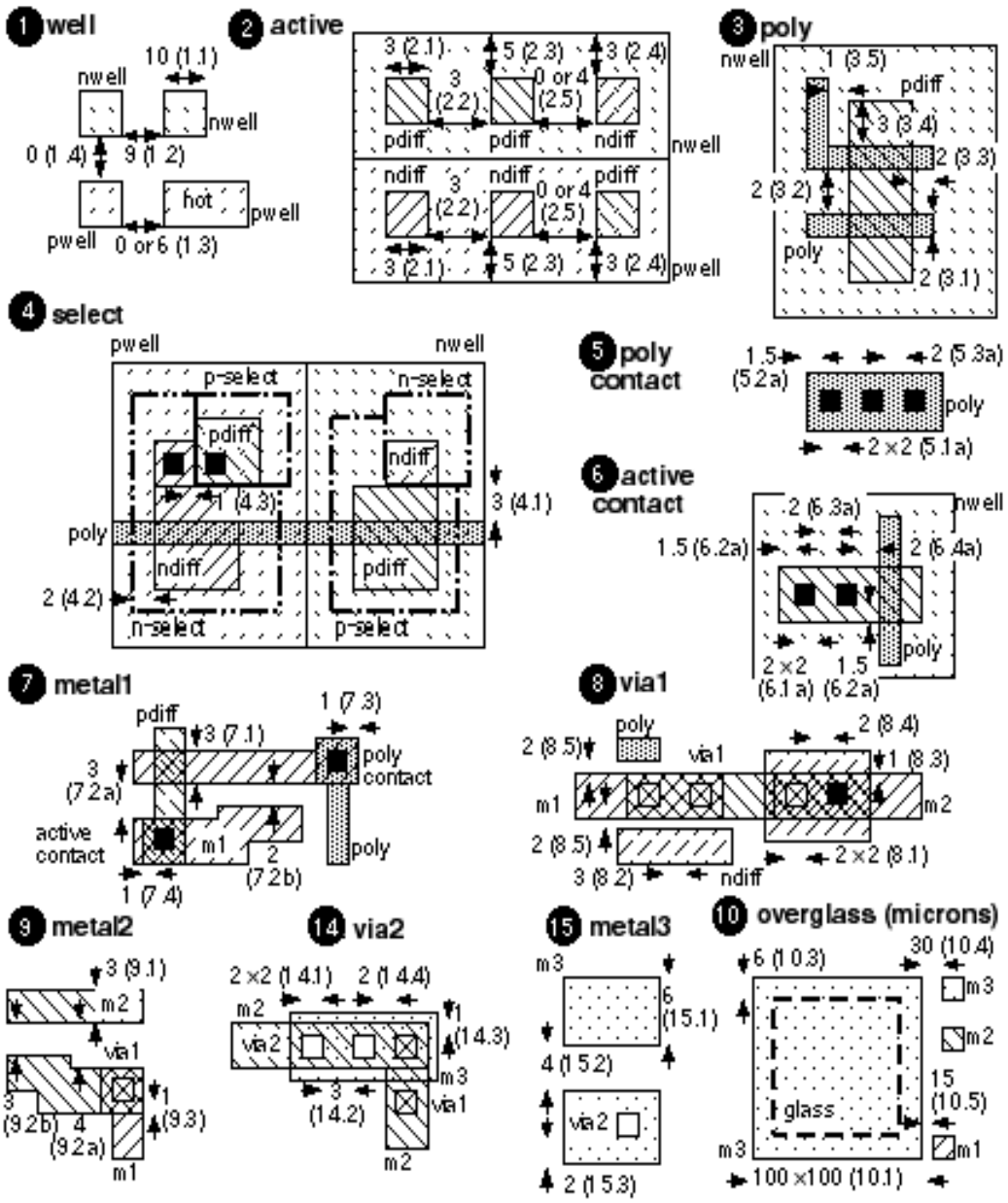
The layout designer must follow these rules in order to guarantee a certain yield for the finished product, i.e., a certain ratio of acceptable chips out of a fabrication batch. A design which violates some of the layout design rules may still result in a functional chip, but the yield is expected to be lower because of random process variations.The design rules below are given in terms of scaleable lambda-rules. Note that while the concept of scaleable design rules is very convenient for defining a technology-independent mask layout and for memorizing the basic constraints, most of the rules do not scale linearly,



especially for sub-micron technologies. This fact is illustrated in the right column, where a representative rule set is given in real micron dimensions. A simple comparison with the lambda- based rules shows that there are significant differences. Therefore, lambda-based design rules are simply not useful for sub-micron CMOS technologies.

CMOS Design Rules:

Figure 2.11 defines the design rules for a CMOS process using pictures. Arrows between objects denote a minimum spacing, and arrows showing the size of an object denote a minimum width. Rule 3.1, for example, is the minimum width of poly (2 l). Each of the rule numbers may have different values for different manufacturers—there are no standards for design rules.



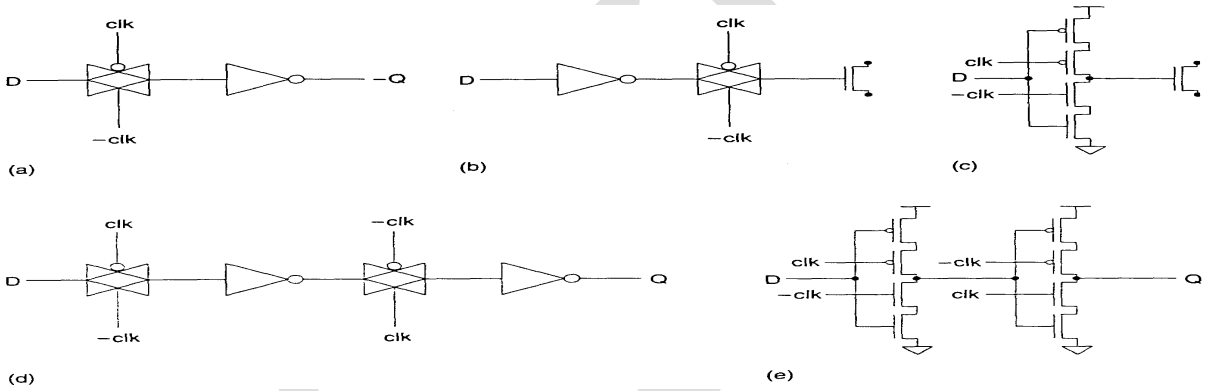
UNIT 3

GATE LEVEL DESIGN

Logic gate is an idealized or physical device implementing a Boolean function, that is, it performs a logical operation on one or more logic inputs and produces a single logic output. Depending on the context, the term may refer to an **ideal logic gate**, one that has for instance zero rise time and unlimited fan-out, or it may refer to a non-ideal physical device.

Switch logic:

Switch logic is based on the pass transistor or on transmission gates. This approach is fast for small arrays and takes no static current from the supply rails. Thus, power dissipation of such arrays is small since current inly fows on switching.



(figure shows transmission gates)

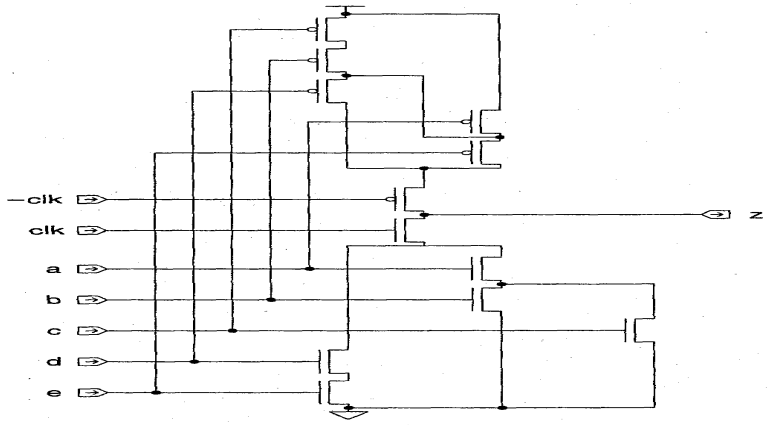
Pass transistors and Transmission gates:

Switches and switch logic ay be formed from simple n or p-pass transistors or from transmission gates comprising an n-pass and a p-pass transistor in parallel the reason for adopting the apparent complexity of the transmission gate, rather than using a simple n-switch or p-switch in most CMOS applications, is to eliminate the undesirable threshold voltage effects which give rise to the loss of logic levels in pass transistors

Other forms of CMOS logic:

Clocked CMOS Logic (C2MOS):

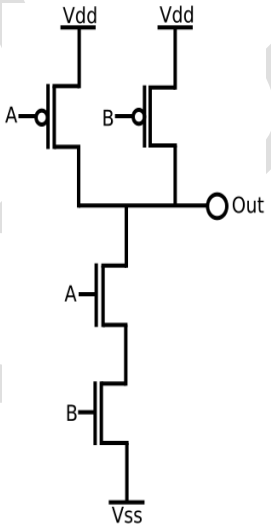
Clocked CMOS logic has been used for very low power CMOS and/or for minimizing hot electron effect problems in N-FET devices .Clocking transistors allow valid logic output only when clk is high. Clocking transistors may be at output end of logic trees (maximum performance) or at power supply end of logic trees (maximum protection from hot electrons)



Pseudo-noms logic:

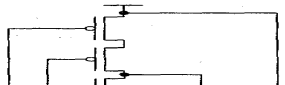
Using a PMOS transistor simply as a pull-up device for an n-block is called pseudo-NMOS logic. Note, that this type of logic is no longer ratio-less, i.e., the transistor widths must be chosen properly, i.e., The pull-up transistor must be chosen wide enough to conduct a multiple of the n-block's leakage and narrow enough so that the n-block can still pull down the output safely.

Dynamic CMOS logic:
The actual logic is implemented in the inherently faster nmos logic, a p-transistor is used for the non-time-critical precharging of the output line so that the output capacitance is charged to V_{dd} during the of period of the clock signal.



Domino CMOS logic

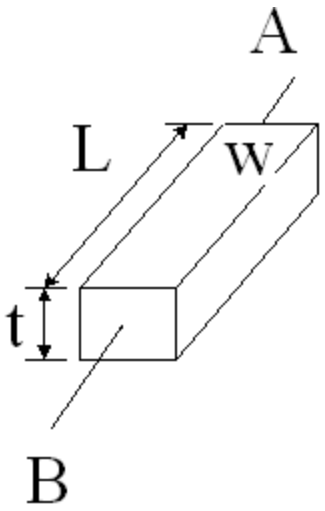
Domino logic is a CMOS-based evolution of the dynamic logic techniques which were based on either PMOS or NMOS transistors. It allows a rail-to-rail logic swing. It was developed to speed up circuits.



In Dynamic Logic, a problem arises when cascading one gate to the next. The precharge "1" state of the first gate may cause the second gate to discharge prematurely, before the first gate has reached its correct state. This uses up the "precharge" of the second gate, which cannot be restored until the next clock cycle, so there is no recovery from this error.

Sheet Resistance:

- Resistance of a square slab of material
- RAB = ρL/A
- => R = ρL/t*W
- Let L = W (square slab)
- => RAB = ρ/t = Rs ohm / square



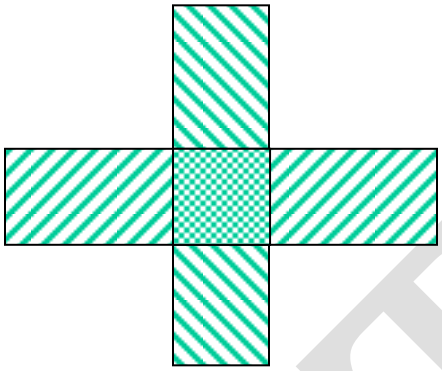
Typical sheet resistance values for materials are very well characterized

Layer	Rs (Ohm / Sq
Aluminium	0.03
N Diffusion	10 – 50
Silicide	2 – 4
Polysilicon	15 - 100
N-transistor Channel	104
P-transistor Channel	2.5 x 104

N-type Minimum Feature Device:

R = 1sq x Rs = Rs = 104 Ω

2λ



Capacitance:

Standard unit for a technology node is the gate - channel capacitance of the minimum sized transistor (2λ x 2λ), given as • Cg .This is a 'technology specific' value.

Delay Unit:

- For a feature size square gate, τ = Rs x • Cg
- i.e. for 5μm technology, τ = 104 ohm/sq x 0.01pF = 0.1ns
- Because of effects of parasitic which we have not considered in our model, delay is typically of the order of 0.2 - 0.3 ns
- Note that τ is very similar to channel transit time τsd .

CMOS Inverter Delay:

- Pull-down delay = Rpd x 2 • Cg
- Pull-up delay = Rpu x 2 • Cg
- Asymmetry in rise and fall due to resistance difference between pull-up and pull-down (factor of 2.5) (due to mobilities of carriers)
- Delay through a pair of inverters is 2 τ (fall time) + 5 τ (rise time)

- Delay through a pair of CMOS inverters is therefore 7 τ.

CMOS Inverter Rise and Fall Time Estimation:

- Tf ~ 3CL / βVDD
- Tr ~ 3CL / βVDD
- (Derivations for the above are in Pucknell and Eshraghian Pages 105 - 107)
- So, τ r/ τf = βn/βp
- Given that (due to motilities) βn = 2.5 βp, rise time is slower by a factor of 2.5 when using minimum dimensions of n and p transistors.

Super Buffers:

The symmetry of the conventional inverter is clearly undesirable, and gives rise to significant delay problems when an inverter is used to drive more significant capacitive loads. Other NMOS arrangements such as those based on the native transistor, and known as native super buffers, may be used.

Unit 4:

DATA PATH SUBSYSTEMS

Large systems are composed of sub-systems, known as Leaf-Cell .The most basic leaf cell is the common logic gate (inverter, and, ..Etc). Structured Design-High regularity-Leaf cells replicated many times and interconnected to form the system. Logical and systematic approach to VLSI design is essential.

SHIFTER:

A Shifter is most widely used for arithmetic operations. usually shifting is equivalent to multiplication by powers of two. Shifting is required during floating-point arithmetic. The shit register is simplest shifters that can shift by one position per clock cycle.

BARREL SHIFTER:

Barrel shifter produces n output bits and accepts 2n data bits , n control signals . The Barrel shifter shifts by transmitting a n-bits slice of the 2n data bits to the output.